WHAT IS CLAIMED

1. A method of regenerating an output clock signal for controlling the coupling of received data to an output port therefor comprising the steps of:

(a) clocking said received data into a first-in, first-out (FIFO) storage buffer in accordance with an input clock signal associated with said received data signal and a data valid signal representative of valid received data;

(b) coupling said input clock signal to a multitap delay line, having outputs that provide respectively different phase delayed versions of said input clock signal;

(c) coupling one of said outputs of said multitap delay line to said output port from which said output clock signal is derived, said output clock signal being coupled to said FIFO storage buffer to clock out data therefrom;

(d) controllably coupling another of said outputs of said multitap delay line to said output port so as to change said output clock signal in accordance with a relationship between said valid data signal and said output clock signal.

2. The method according to claim 1, wherein step (d) comprises controllably coupling to said output port an output of said multitap delay line that provides a later-in-time delay relative to said one of said outputs of said multitap delay line, in response to said output clock

signal exhibiting a clock frequency that is higher than the effective frequency of said valid data signal, thereby reducing the frequency of said output clock signal.

3. The method according to claim 1, wherein step (d) comprises controllably coupling to said output port an output of said multitap delay line that provides an earlier-in-time delay relative to said one of said outputs of said multitap delay line, in response to said output clock signal exhibiting a clock frequency that is lower than the frequency of said valid data signal, thereby increasing the frequency of said output clock signal.

4. The method according to claim 1, wherein said relationship between said valid data signal and said output clock signal is represented by the amount of data contained in said FIFO storage buffer and the data storage capacity of said FIFO storage buffer.

5. The method according to claim 4, wherein said relationship between said valid data signal and said output clock signal is represented by an underflow or overflow condition of said FIFO storage buffer.

6. The method according to claim 5, wherein step (d) comprises controllably coupling to said output port an output of said multitap delay line that provides a later-

in-time delay relative to said one of said outputs of said multitap delay line, in response to said output clock signal causing an underflow condition of said FIFO storage buffer, thereby reducing the frequency of said output clock signal.

7. The method according to claim 5, wherein step (d) comprises controllably coupling to said output port an output of said multitap delay line that provides an earlier-in-time delay relative to said one of said outputs of said multitap delay line, in response to said output clock signal causing an overflow condition of said FIFO storage buffer, thereby increasing the frequency of said output clock signal.

8. An apparatus for regenerating an output clock signal for controlling the coupling of received data to an output port therefor comprising:

a first-in, first-out (FIFO) storage buffer into which said received data is clocked in accordance with an input clock signal associated with said received data signal and a data valid signal representative of valid received data;

a multitap delay line to which said input clock signal is coupled, said multitap delay line having outputs that provide respectively different phase delayed versions of said input clock signal; and

a multiplexer, which is controllably operative to couple a selected one of said outputs of said multitap delay line to said output port from which said output clock signal is derived, in accordance with a relationship between said valid data signal and said output clock signal.

9. The apparatus according to claim 8, wherein said multiplexer is operative to controllably couple to said output port an output of said multitap delay line that provides a later-in-time delay relative to said selected one of said outputs of said multitap delay line, in response to said output clock signal exhibiting a clock frequency that is higher than the effective frequency of said valid data signal, thereby reducing the frequency of said output clock signal.

10. The apparatus according to claim 8, wherein said multiplexer is operative to controllably couple to said output port an output of said multitap delay line that provides an earlier-in-time delay relative to said selected one of said outputs of said multitap delay line, in response to said output clock signal exhibiting a clock frequency that is lower than the frequency of said valid data signal, thereby increasing the frequency of said output clock signal.

11. The apparatus according to claim 8, wherein said relationship between said valid data signal and said output clock signal is represented by the amount of data contained in said FIFO storage buffer and the data storage capacity of said FIFO storage buffer.

12. The apparatus according to claim 11, wherein said relationship between said valid data signal and said output clock signal is represented by an underflow or overflow condition of said FIFO storage buffer.

13. The apparatus according to claim 12, wherein said multiplexer is operative to controllably couple to said output port an output of said multitap delay line that provides a later-in-time delay relative to said one of said outputs of said multitap delay line, in response to said output clock signal causing an underflow condition of said FIFO storage buffer, thereby reducing the frequency of said output clock signal.

14. The apparatus according to claim 12, wherein said multiplexer is operative to controllably couple to said output port an output of said multitap delay line that provides an earlier-in-time delay relative to said one of said outputs of said multitap delay line, in response to said output clock signal causing an overflow condition of

said FIFO storage buffer, thereby increasing the frequency of said output clock signal.

15. An apparatus for regenerating an output clock signal for controlling the coupling of received data to an output port therefor comprising:

a first-in, first-out (FIFO) storage buffer into which said received data is clocked in accordance with an input clock signal associated with said received data signal and a data valid signal representative of valid received data;

a fixed fractional delay line having an input port coupled to receive said input clock signal, said fixed fractional delay line having a plurality of outputs that provide respectively different phase delayed versions of said fixed frequency input clock signal;

a multiplexer having a plurality of inputs respectively coupled to said plurality of outputs of said fixed fractional delay line, and being controllably operative to couple one of said outputs of said fixed fractional delay line to said output port; and

a control loop coupled with said FIFO storage buffer, said output port and a steering control input of said multiplexer circuit, and being operative to selectively change which of said outputs of said fixed fractional delay line is coupled by said multiplexer to said output port, so as to controllably change said output clock signal in accordance with a relationship between valid data signal

and said output clock signal, and thereby cause the output clock signal to track the effective frequency of the valid data signal.

16. The apparatus according to claim 15, wherein said multiplexer is operative to controllably couple to said output port an output of said fixed fractional delay line that provides a later-in-time delay relative to said selected one of said outputs of said fixed fractional delay line, in response to said output clock signal exhibiting a clock frequency that is higher than the effective frequency of said valid data signal, thereby reducing the frequency of said output clock signal.

17. The apparatus according to claim 15, wherein said multiplexer is operative to controllably couple to said output port an output of said fixed fractional delay that provides an earlier-in-time delay relative to said selected one of said outputs of said fixed fractional delay line, in response to said output clock signal exhibiting a clock frequency that is lower than the frequency of said valid data signal, thereby increasing the frequency of said output clock signal.

18. The apparatus according to claim 15, wherein said relationship between said valid data signal and said output clock signal is represented by the amount of data contained

in said FIFO storage buffer and the data storage capacity of said FIFO storage buffer.

19. The apparatus according to claim 18, wherein said multiplexer is operative to controllably couple to said output port an output of said fixed fractional delay line that provides a later-in-time delay relative to said one of said outputs of said fixed fractional delay line, in response to said output clock signal causing an underflow condition of said FIFO storage buffer, thereby reducing the frequency of said output clock signal.

20. The apparatus according to claim 18, wherein said multiplexer is operative to controllably couple to said output port an output of said fixed fractional delay line that provides an earlier-in-time delay relative to said one of said outputs of said fixed fractional delay line, in response to said output clock signal causing an overflow condition of said FIFO storage buffer, thereby increasing the frequency of said output clock signal.